## REMARKS

### Summary of Claim Status

Claims 1-31 are pending in the present application after entry of the present amendment. Claims 1-17 and 22-31 are rejected for the reasons discussed below. Claims 18-21 are withdrawn.

Applicant requests the favorable reconsideration of the claims and withdrawal of the pending rejections and objections, in view of the following remarks.

### Rejections Under 35 USC 102(b)

Claims 1-17 and 22-31 are rejected as being anticipated by de Lima ("Designing Single Event Upset Mitigation Techniques for Large SRAM-based FPGA Devices", Thesis Proposal; Porto Alegre, February 11, 2002). Applicants respectfully traverse this rejection with regard to all claims.

The Office Action states, in part:

> As to claims 1, 8, 10, 12, 20, 22, 28 and 30 de Lima Discloses:
>
> ...
>
> identifying first and second data input terminals of a programmable routing multiplexer in the PLD (A voter (or majority circuit) is implemented by the top MUX to create a "hardened" output ... terminals D, G - fig. 2.6, page 18), wherein a selection between the first and second data input terminals is determined by a first value stored in a first memory cell controlling the programmable routing multiplexer (if both A and B read logic zero, MUX input D0 is selected - page 18) (pages 18, 25, 53-54);
>
> routing the node on a first routing path between the first and second logic blocks, wherein the first routing path traverses the programmable routing multiplexer via the first data input terminal (if A and B disagree due to an SEU (or for other reasons), the MUX will select flip-flop C. We know C agrees with either A or B, and thus the MUX "voted" to produce data agreed on by two of the three flip-flops - page 18); and
>
> routing the node on a second routing path between the first and second logic blocks, wherein the second routing path traverses the programmable routing multiplexer via the second data input terminal (if A and B disagree due to an SEU (or for other reasons), the MUX will select flip-flop C. We know C agrees with either A or B, and thus the MUX "voted" to produce data agreed on by two of the three flip-flops - page 18). *(emphasis original)*

The Office Action cites Figure 2.6 on page 18 of de Lima, which is a TMR (triple modular redundancy) circuit. In this circuit, a value D is stored in three flip-flops, and the outputs of the flip-flops are "voted" on, where any value stored in at least two of the flip-flops is provided as the output Q of the circuit. Such circuits are well known, and Applicants do not dispute the prevalence of TMR circuits in the art of PLD design implementation.

However, the claimed invention is not a TMR circuit. In fact, as shown by Claims 7, 9, 11, 17, 19, 21, 27, 29, and 31, the claimed methods can include an evaluation step to determine that the circuit is not a TMR circuit, e.g., prior to implementing the other steps. Therefore, the claimed invention can be used as an alternative to the TMR approach.

In Applicants' claimed methods, during implementation of a design in the PLD, a single node ("the node") is routed on two different paths through the same multiplexer ("the programmable routing multiplexer"), using two different data input terminals of the multiplexer ("the first and second data input terminals"). A selection between the two input paths is controlled solely by a value stored in a memory cell controlling the multiplexer ("the first memory cell"); and thus potentially subject to single event upset (SEU). However, because the selection is controlled solely by the contents of the one memory cell, such an SEU will merely change the selection from one of the paths to the other (e.g., from the first routing path to the second routing path, or *vice versa*), and they each provide the same input signal to the multiplexer on a different data input terminal. Thus, an SEU that incorrectly changes the select function of the multiplexer by changing the value stored in the select memory cell still leaves the multiplexer providing the correct output signal.

De Lima neither teaches nor suggests this SEU mitigation technique. Specifically, de Lima neither teaches nor suggests Applicants' claimed:

> identifying first and second data input terminals of a programmable routing multiplexer in the PLD, wherein a selection between the first and second data input terminals is determined solely by a first value stored in a first memory cell controlling the programmable routing multiplexer;
>
> routing the node on a first routing path between the first and second logic blocks, wherein the first routing path traverses the

programmable routing multiplexer via the first data input terminal; and

routing the node on a second routing path between the first and second logic blocks, wherein the second routing path traverses the programmable routing multiplexer via the second data input terminal. (Claims 1, 8, and 10)

or Applicants' claimed:

routing the PLD placement to generate a routed design wherein the node is routed on a first routing path between the first and second logic blocks, the first routing path traversing a programmable routing multiplexer via a first data input terminal of the programmable routing multiplexer;

identifying a second data input terminal of the programmable routing multiplexer, wherein a selection between the first and second data input terminals is determined solely by a first value stored in a first memory cell controlling the programmable routing multiplexer; and

routing the node on a second routing path between the first and second logic blocks, wherein the second routing path traverses the programmable routing multiplexer via the second data input terminal. (Claim 12)

or Applicants' claimed:

a routing module for routing the PLD placement to generate a routed design wherein the node is routed on a first routing path between the first and second logic blocks, the first routing path traversing a programmable routing multiplexer via a first data input terminal of the programmable routing multiplexer; and

a post-processing module for:

identifying a second data input terminal of the programmable routing multiplexer, wherein a selection between the first and second data input terminals is determined solely by a value stored in a memory cell controlling the programmable routing multiplexer, and

routing the node on a second routing path between the first and second logic blocks, wherein the second routing path traverses the programmable routing multiplexer via the second data input terminal. (Claim 20)

or Applicants' claimed:

identifying in a programmable routing multiplexer of the PLD a first data input terminal and a second data input terminal, wherein a selection between the first and second data input terminals is determined solely by a first value stored in a first memory cell controlling the programmable routing multiplexer;

routing a node in the design to the first data input terminal; and routing the node to the second data input terminal. (Claim 22)

or Applicants' claimed:

[code/identification module] for identifying in a programmable routing multiplexer of the PLD a first data input terminal and a second data input terminal, wherein a selection between the first and second data input terminals is determined solely by a first value stored in a first memory cell controlling the programmable routing multiplexer; and [code/routing module] for routing a node in the design to both of the first and second data input terminals. (Claims 28 and 30)

Therefore, and for at least these reasons, Claims 1, 8, 10, 12, 20, 22, 28 and 30 are allowable over de Lima. Further, Claims 2-7, 9, 11, 13-17, 21, 23-27, 29, and 31-34 are allowable for at least the reasons of Claims 1, 8, 10, 12, 20, 22, 28 and 30, from which they depend.

Applicants must also respectfully note that the rejection of Claims 7, 9, 11, 17, 27, 29, and 31 included in the Office Action is inadequate. These claims specify that the method/program/system further comprises evaluating the source and destination logic (or node) and determining that the source and destination logic (or node) do not form a portion of a triple modular redundancy (TMR) circuit. Clearly, since de Lima's circuit is a TMR circuit (see the paragraph immediately above de Lima's Figure 2.6 on page 18), de Lima neither teaches nor suggests this feature of the claims. Therefore, Claims 7, 9, 11, 17, 27, 29, and 31 further distinguish over de Lima for at least this additional reason.

If the rejection of Claims 7, 9, 11, 17, 27, 29, and 31 is maintained, Applicants respectfully request that this feature of the claims be addressed in its entirety.

Conclusion

No new matter has been introduced by any of the above amendments. All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested. If any action other than allowance is contemplated by the

Examiner, the Examiner is respectfully requested to telephone Applicants' agent, Lois D. Cartier, at 720-652-3733.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as **first class mail** in an envelope addressed to: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450, on July 5, 2007.

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